Lab 5 Report
ECE1212 Electronic Circuits Design Lab
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Introduction

More than 99% of all ICs are MOSFETs used for random-access memory, flash memory, processors, application-specific integrated circuits, and other applications. Furthermore, in the year 2000, 10^6 MOSFETs per person per year were manufactured. All MOSFETs are transistors that consist of metal, oxide, and a semiconductor (usually Si).

The basic principle of the MOSFET is that the source to drain current is controlled by the gate voltage. The electric field of the gate induces charge in the semiconductor at the semiconductor-oxide interface. Therefore, the MOSFET is a voltage-controlled current source.

In this experiment the goal was to make use of the CD4007 MOSFET array. The array consists of six transistors, three p-channel and three n-channel, interconnected to some extent in order to reduce the number of IC pins required. Through implementation of this MOSFET array, students were tasked with designed a current mirror which would then bias a common-source nMOSFET amplifier circuit.

Procedure

Part A: Design of a Current Mirror

(1) In the prelab, students designed two current mirror circuits based on measurements with the curve tracer, selecting a $I_{D,LOW}$ = 1mA target current and an $I_{D,HIGH}$ = 4mA target current for the current mirror. Choosing V_{DD} as 15V, students calculated the resistance R_M in both cases to be:

$$R_{M_LOW} = 12k + 180 = 12.18k\Omega$$
$$R_{M_HIGH} = 2.4k + 220 = 2.62k\Omega$$

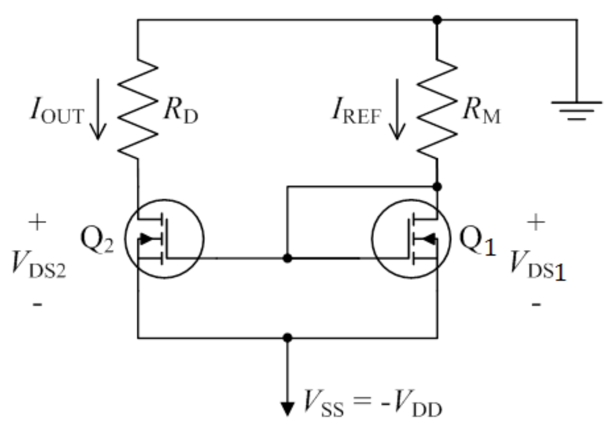

Figure 1: Circuit Schematic of Current Mirror

(2) Students then constructed the current mirror circuit according to the figure above. Starting with the drain current in transistor Q1 as $I_{REF} = I_{D,HIGH}$ = 4mA, the circuit was constructed with $R_M = R_{M,HIGH}$ = 2.62kΩ.

(3) Using a decade box to set $R_D = R_M$ and applying voltage to the circuit, students measured the voltages V_{SS}, V_{DS1}, and V_{DS2} and computed the currents I_{REF} and I_{OUT}, confirming the current mirror was functioning as intended.

(4) The resistance of the decade box was then varied so that R_D took on each of the values: $R_D = 0.2R_M$, $0.3R_M$,..., $0.9R_M$, $1.0R_M$, $1.5R_M$, $2.0R_M$,..., $4.5R_M$, $5.0R_M$. For each resistance, V_{DS2} was measured and

I_{OUT} was calculated.

(5) A plot was made showing V_{DS2} and I_{OUT} vs. R_D.

(6) Steps (2-5) were repeated for $I_{REF} = I_{D,LOW} = 1$mA.

Part B: Common-Source nMOSFET Amplifier Biased by a Current Mirror

(1) In the prelab, students performed both DC and AC analyses of the Common-Source Amplifier circuit to design for -5V gain and signal smoothing with capacitors. This was repeated for both operating points $I_{D,LOW} = 1$mA and $I_{D,HIGH} = 4$mA. Other circuit design considerations were discussed. Ultimately, $I_{D,LOW}$ was chosen to for the amplifier circuit design moving forward.

(2) The circuit was constructed according to the prelab design, without any capacitors. The voltage drop across each resistor was measured to compare against theoretical calculations.

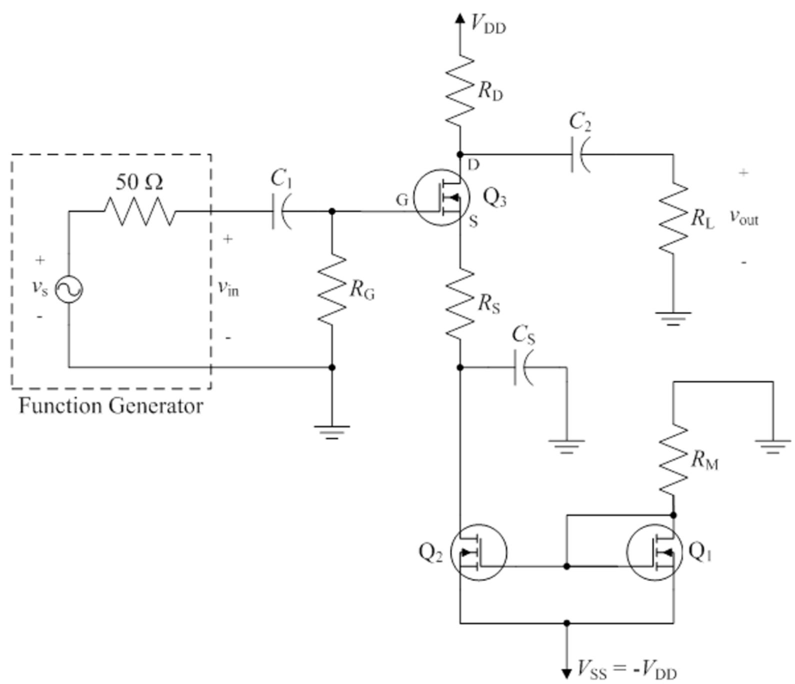

Figure 2: Circuit Schematic of Common-Amplifier driven by Current Mirror

(3) The gate and drain voltages V_{GS} and V_{DS} of each of the transistors was measured to confirm that the circuit was wired and functioning correctly.

(4) The calculated capacitors were added to the circuit, and the system gain in response to a rough sweep of 1kHz low-amplitude sinusoid inputs. The oscilloscope acted as the circuit load.

(5) The precise value of R_s was changed to precisely tune the gain to as close as possible to 5V/V.

(6) The 3dB bandwidth of the circuit was measured by finding both 70.7% drop off points on either side of the 1kHz input signal.

(7) A myriad of questions and circuit design consequences were discussed, including a discussion of the classes overall Lab experiences.

Results

Part A: Design of a Current Mirror

(1 and 2) Students first constructed the current mirror circuit with $I_{D,HIGH}$ = 4mA, using the R_M = $R_{M,HIGH}$ = 2.62kΩ resistor.

(3) Letting $R_D = R_M$, the voltages V_{SS}, V_{DS1}, and V_{DS2} were measured to calculate I_{REF} and I_{OUT} in order to confirm that the current mirror functioned properly with I_{OUT} approximately equal to I_{REF}. The results are shown in the table below.

Measured	V	Calculated	A
V_{SS}	-14.987	I_{out}	0.00384
V_{DS2}	4.925	I_{ref}	0.00402
V_{DS1}	4.464		

Table 1: Voltage measurements and current calculations of current mirror circuit with $R_D = R_M$

(4) The resistance of the decade box was then varied so that R_D took on each of the values multiple values above and below R_M. For each resistance, V_{DS2} was measured and I_{OUT} was calculated. The data is summarized in the table below.

Factor of R_M	R_D	V_{DS2}	I_{OUT}
0.2	524	12.756	0.00426
0.3	786	11.767	0.00410
0.4	1048	10.815	0.00398
0.5	1310	9.812	0.00395
0.6	1572	8.816	0.00393
0.7	1834	7.824	0.00391
0.8	2096	6.842	0.00389
0.9	2358	5.875	0.00386
1	2620	4.928	0.00384
1.5	3930	1.503	0.00343
2	5240	0.935	0.00268
2.5	6550	0.703	0.00218
3	7860	0.566	0.00183
3.5	9170	0.475	0.00158
4	10480	0.41	0.00139
4.5	11790	0.36	0.00124
5	13100	0.322	0.00112

Table 2: Voltage measurements and current calculations of current mirror circuit with R_D varied for $I_{D,HIGH}$

(5) A plot was made showing V_{DS2} and I_{OUT} vs. R_D for I_{REF} = 4mA.

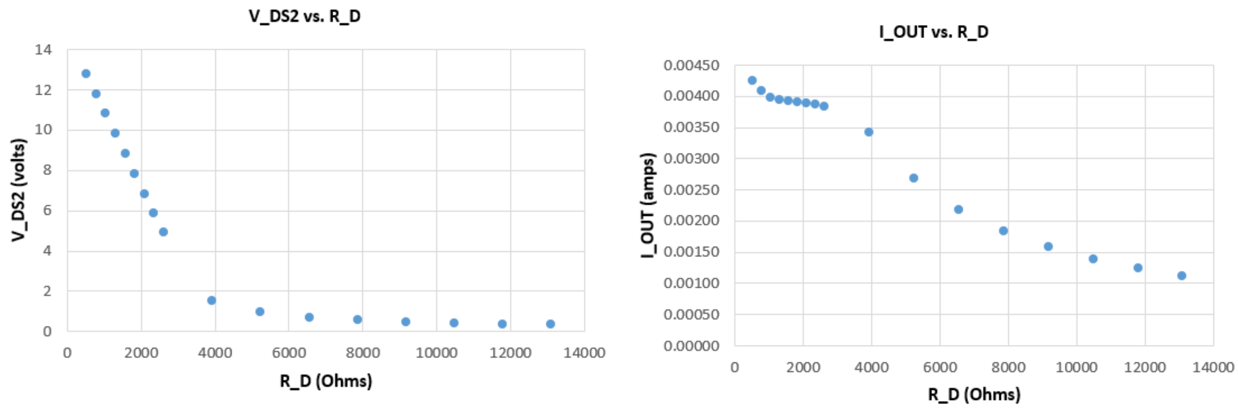

Figure 3: V_{DS} (left) and I_{OUT} (right) vs. R_D for $I_{REF} = I_{D,HIGH} = 4mA$

(6) Steps (2-5) were repeated for $I_{REF} = I_{D,LOW} = 1mA$

Measured	V	Calculated	A
V_{SS}	-14.996	Iout	0.00099
V_{DS2}	2.993	Iref	0.001
V_{DS1}	2.805		

Table 3: Voltage measurements and current calculations of current mirror circuit with $R_D = R_M$ for $I_{D,LOW}$

Factor of R_M	R_D	V_{DS2}	I_{OUT}
0.2	2436	12.439	0.00105
0.3	3654	11.205	0.00104
0.4	4872	9.973	0.00103
0.5	6090	8.764	0.00102
0.6	7308	7.571	0.00102
0.7	8526	6.382	0.00101
0.8	9744	5.226	0.001
0.9	10962	4.086	0.001
1	12180	2.994	0.00099
1.5	18270	0.535	0.00079
2	24360	0.344	0.0006
2.5	30450	0.259	0.00048
3	36540	0.209	0.0004
3.5	42630	0.175	0.00035
4	48720	0.151	0.0003
4.5	54810	0.133	0.00027
5	60900	0.118	0.00024

Table 4: Voltage measurements and current calculations of current mirror circuit with R_D varied for $I_{D,LOW}$

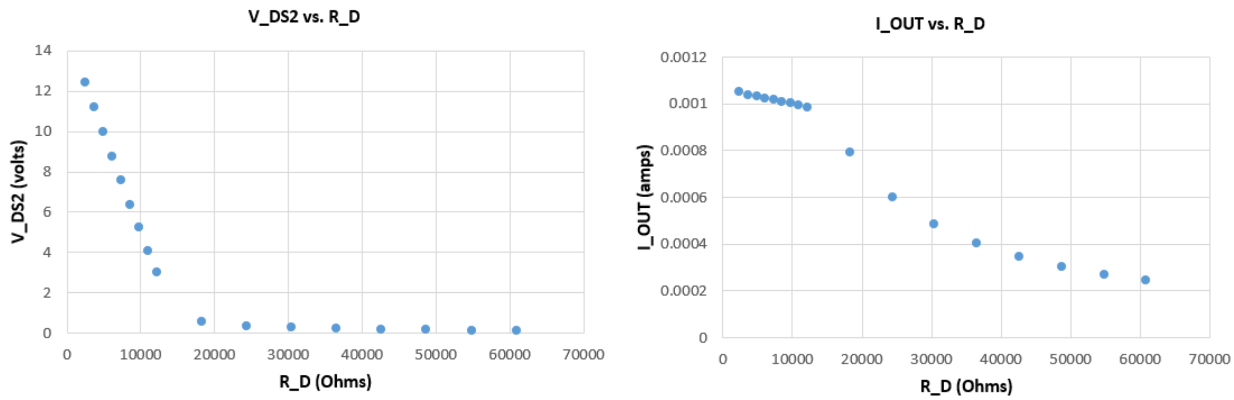

Figure 4: V_DS (left) and I_{OUT} (right) vs. R_D for $I_{REF} = I_{D,LOW} = 1mA$

Part B: Common-Source nMOSFET Amplifier Biased by a Current Mirror

(1) $I_{D,LOW}$ circuit design was chosen to for the amplifier circuit, meaning resistors values:

$$R_D = 7500\Omega$$
$$R_S = 750\Omega$$
$$R_G = 9M\Omega$$
$$R_M = 12180\Omega$$

The design values could all be easily achieved with one or two resistors, while R_G was achieved with a decade box.

(2) Below is a table of the voltage drops and currents across the circuit resistors:

Transistor	V_{drop} (V)	R-val (Ω)	R-name (Ω)	I_D (A)
Q1	12.181	12180	R_M	0.001000082102
Q2	0.764	750	R_S	0.001018666667
Q3	7.656	7500	R_D	0.0010208

Table 5: Common-Source Amplifier Circuit Calculated Currents

The resulting currents were all within 2% of the designed operating current of 1mA. This confirms that the circuit works correctly according to design specifications.

(3) Below is a table of the drain and gate voltages of each transistor:

Transistor	V_{DS} (V)	V_{GS} (V)
Q1	2.815	2.815
Q2	6.98	2.815
Q3	14.582	5.655

Table 6: Common-Source Amplifier Circuit Drain-Source and Gate-Source Voltages

All voltages drops were as expected and will be discussed in the next section.

(4 and 5) Below is a table of output RMS values and their associated gains in response to a rough sweep of input RMS voltages:

Input RMS (V)	Ouput RMS (V)	Gain
0.0188	0.0895	4.760638298
0.0405	0.193	4.765432099
0.0592	0.292	4.932432432
0.0791	0.39	4.930467762
0.0959	0.48	5.005213764

Table 7: Calculated Gain for Various Input Voltages

The input voltages were ≈ 20, 40, 60, 80, and 100mV. R_S had been tuned to 593Ω so that the gain of the 100mV input was -5V, shown below:

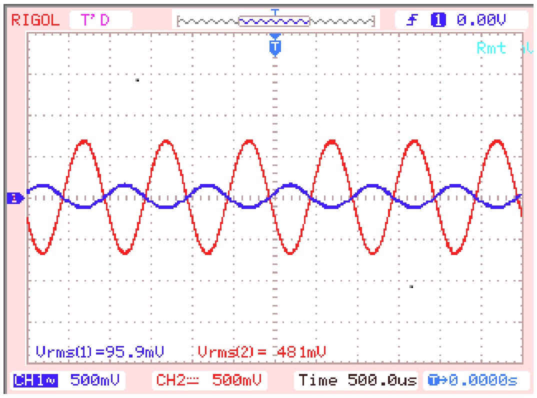

Figure 5: Output in response to 95.9mVRMS input

(6) Below is a table of the 3dB bandwidth measurements:

	Output RMS (V)	f (Hz)
Output	0.48	1000
0.707 below	0.33936	50
0.707 above	0.33936	400000

Table 8: This table displays the values measured to determine the 3dB bandwidth of the circuit

The difference between the ±0.707 frequencies yielded a 3dB bandwidth of 399.95kHz.

(7) See next section for circuit discussions.

Discussion

Part A: Design of a Current Mirror

(1 and 2) The circuit was constructed following the procedure starting with $I_{REF} = I_{D,HIGH} = 4mA$.

(3) The current mirror currents that were calculated based on the measurements of voltages were $I_{REF} = 4.02mA$ and $I_{OUT} = 3.84mA$. With an intended reference current of 4mA, this resulted in a 0.5% error of the measured I_{REF} to the intended reference current, a 4% error of the measured I_{OUT} to the intended reference current, and a 4.48% error of the measured I_{OUT} to the measured I_{REF} current which were intended to match. With all of these current comparisons under 5% error, we could confidently confirm that our current mirror was functioning properly.

(4) In part (4) of the results section of part A, the output current was measured and calculated after varying R_D. As seen in the table, as R_D increases, the voltage drop across the resistor R_D increases, which in turn makes the voltage V_{DS2} decrease. As this drain to source voltage dropped, we see that eventually, I_{OUT} begins to fall below the desired 4mA and eventually drops all the way down to 1mA. This is expected because at 4mA, the MOSFET is operating in the saturation region. As V_{DS2} drops, eventually the MOSFET falls out of the saturation region at the point where $V_{DS2} = V_{GS} - V_T$. Below this point, the current drops as the MOSFET leaves saturation and goes back into the triode region.

(5) As seen in the plots from Figure 3, the point where $R_D = R_M$ is at 2620Ω. In both plots, it is easily seen the significant change between either side of this resistance. In the voltage plot, V_{DS2} linearly decreases as the resistance increases, and the MOSFET is still in the saturation region, which is reflected with a consistent output current of about 4mA shown in the current plot on the right. Once the resistance is greater than R_M, both plots then change drastically. The drain to source voltage levels off as it approaches zero because the resistor continues to drop more voltage across it. Consequently, in the corresponding current plot, the current begins to drop off once the resistor is greater than R_M. This again is expected because we have left the saturation region and are entering the triode region.

(6) In the case of $I_{D,LOW}$ = 1mA, the current mirror currents that were calculated based on the measurements of voltages were I_{REF} = 1mA and I_{OUT} = 0.99mA. With an intended reference current of 1mA, this resulted an approximately 0% error of the measured I_{REF} to the intended reference current, a 1% error of the measured I_{OUT} to the intended reference current, and a 1% error of the measured I_{OUT} to the measured I_{REF} current which were intended to match. With all of these current comparisons under 1% error, we could confidently confirm that our current mirror was functioning properly.

In part (6) of the results section of part A, the output current was measured and calculated after varying R_D. Similarly to the previous circuit where I_{REF} = 4mA as seen in the table, as R_D increases, the voltage drop across the resistor R_D increases, which in turn makes the voltage V_{DS2} decrease. As this drain to source voltage dropped, we see that eventually, I_{OUT} begins to fall below the desired 1mA and eventually drops all the way down to 0.24mA. This is expected because at 1mA, the MOSFET is operating in the saturation region. As V_{DS2} drops, eventually the MOSFET falls out of the saturation region at the point where $V_{DS2} = V_{GS} - V_T$. Below this point, the current drops as the MOSFET leaves saturation and goes back into the triode region.

As seen in the plots from Figure 4, the point where $R_D = R_M$ is at 12180Ω. In both plots, it is easily seen the significant change between either side of this resistance similarly to the plots of the high reference current in Figure 3. In the voltage plot, V_{DS2} linearly decreases as the resistance increases, and the MOSFET is still in the saturation region, which is reflected with a consistent output current of about 1mA shown in the current plot on the right. Once the resistance is greater than R_M, both plots then change drastically again. The drain to source voltage levels off as it approaches zero because the resistor continues to drop more voltage across it leaving less to drop from drain to source. In the corresponding current plot, the current begins to drop off once the resistor is greater than R_M. This again is expected because we have left the saturation region and are entering the triode region.

(7) To summarize, as the resistance is below the point where $R_D = R_M$, the current mirror works well because the MOSFETs are well within the saturation region where V_{DS} is greater than $V_{GS} - V_T$. When R_D increases above R_M, the current mirror doesn't work well because the MOSFETs start to leave the saturation region and enter the triode region resulting in a drop in current.

Part B: Common-Source nMOSFET Amplifier Biased by a Current Mirror

(1 and 2) As mentioned in the prelab, in calculating the results for $I_{D,Low}$, the resulting impedance was comfortably positive even with keeping the source voltage at 15V. This is more desirable because the MOSFETs are only rated for so high (18V) source voltage. Any higher drain current would have required a raising of the source voltage to avoid negative impedance.

No AC signal was applied to the circuit during DC bias testing, so the capacitors were not needed (values can be found in the prelab if needed). They were added during the gain testing.

All values experimental values were very close to the designed for values. All drain currents were calculated to be within 2% of the nominal 1mA, and the drop across each transistor was within 1% of the values predicted in the prelab. See Table 5 for results.

(3) As predicted, Q1 and Q2 had the same gate voltages because they were linked in the current mirror, while Q3's gate voltage depended on the input voltage source. The drain voltages were the greatest in descending order from Q3 to Q1. This is reasonable as the respective drain resistors ranked in the same order. See Table 6 for results.

(4 and 5) Table 7 shows that the gain became slightly more accurate for larger inputs from 18.8mV to 9.59mV in intervals of 20mV. A possible explaination is that while lower inputs are usually more accurate due to theoretical output parameters being within operating limits. However, the first several inputs may be so low that noise is a non-negligible component of the signal.

The gain was finely tuned to be within 0.5% of the desired value of -5V by altering R_S from 750Ω to 593Ω. The gain shared an inverse relationship with R_S. See Figure 5 for final input-output oscilloscope image.

(6) The circuit acted as a bandpass filter, with 3dB bandwidth of 399.95kHz, ranging from 50 to 400kHz (See Table 8 for data). On a logarithmic scale, this is shown to be similar to bandpass behaviour. Results were confirmed using DCA pro sweep analysis. Several sources online state that the typical range for an audio signal is from 20-20,000Hz, so the circuit could be used to amplify an audio signal except for the very lowest of frequencies. However, video amplifiers require a significantly higher ceiling frequency in the MegaHz, therefore this circuit would not be suitable to amplify video signals.

(7) According to the gain equation, g_m my be negligible if R_S is large enough. This is desirable as R_S is a tunable parameter and can be precisely controlled. Other circuit design parameters could still be easily met with little modification, as it would require in increase in R_D and R_G to maintain the same gain. It would be a problem if they had to decrease, as it would result in an upper limit on R_S to keep positive impedance for R_D and R_G

Because g_m is an implicit value to specific transistors, the results would also be much more replicable on a larger scale (quantity wise) as the circuit output parameters would depend more on external controllable values (the resistors). Impedance tolerance is much more easily accountable for and fixable than major discrepancies in transconductance.

For the reasons above, Group 26 had the most reliable circuit design, as their R_S was the highest at 1.8kΩ. All other groups had R_S values in the 700Ω range.

Conclusion

The purpose of lab 5 was to experimentally test MOSFET amplifier circuits. The experiments of the lab included designing and testing a current mirror circuit and then using the current mirror circuit to bias a common-source nMOSFET amplifier circuit. The final circuit was also then tested and evaluated. Specifically, the effect of varying the output resistor in the current mirror, the effect of lowering the drain to source voltage out of the saturation region, frequency response, and biasing an amplifier circuit with a current mirror to determine the gains were explored in the lab.

Results accurately reflected what was expected and taught in lecture. Key takeaways were learning the structure and usage of nMOSFET IC CD4007. The laboratory taught how to use nMOSFETS to create two of the most prolific circuits in modern electronics today - current mirrors and common amplifiers. This experiment also demonstrated the importance of accuracy in design to obtain desired results and the differences that can arise between theoretical and practical responses.

References

[1] Experiment 5 – MOSFET Amplifiers and Current Mirrors Lecture Notes

[2] Rigol DM3058 User's Guide. https://www.csulb.edu/sites/default/files/groups/college-of-engineering/About/rigol-dm3058-digital-multimeter-user-guide.pdf

[3] CD4007UB Data Sheet from course website

[4] Professor Li

[5] Curve Tracer User Manual