Lab 7 Report
ECE1212 Electronic Circuits Design Lab
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In this experiment, students studied analog-digital conversion techniques. A "R-2R" D/A converter circuit was both built and evaluated for performance. Additionally, an A/D converter was made using a system of comparators and combinational logic. Both circuits are shown below:

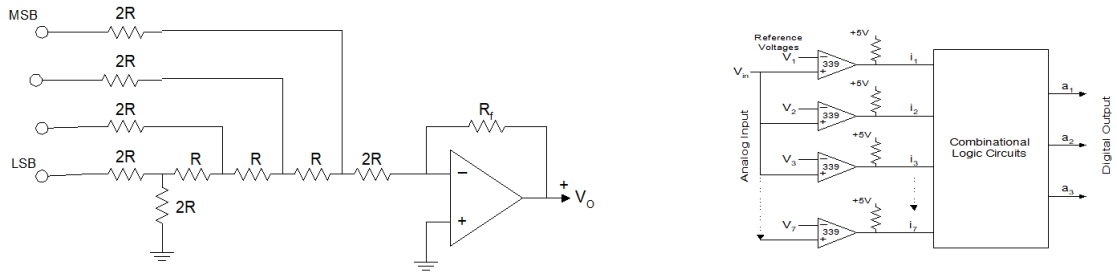

Figure 1: Schematics for both A/D (left) and D/A (right) converters

Students combined both circuits and digital logic knowledge in order to design, implement, and test the circuit, mapping out 15 binary states to their respective input or output voltages.

Procedure

Part A: D/A Conversion with R-2R Ladder Converter

(1) In the prelab, students analyzed the R-2R ladder D/A converter and designed the operational amplifier circuit including the other resistances to achieve a maximum output voltage scaled to 3V. Then, students constructed the R-2R ladder D/A converter according to Figure 1.

(2) The students then estimated V_{off} and G in the following equation by plotting the measured V_{out} versus W (16 points) and finding the best-fit line.

$$V_{out} = V_{off} + G * W$$

(3) Students then compared the errors between the best-fit line and the actual values.

(4) Finally, students observed and recorded the effects of increased counter clock rate on the relative linearity and time response of each D/A. The worst case input transition for the D/A and worst case settling time for the D/A was determined.

Part B: Parallel A/D Converter

(1) In the prelab, students designed a basic voltage divider to input specific voltages into a network of comparators. Combinational logic was designed in logisim to realize the 3bit parallel A/D converter shown in figure 1 The minimal amount of chips were used.

(2) The students verified that the A/D conversion worked using a low-frequency ramp voltage as an analog input and observe the change in the digital output as the ramp varies between zero and five volts.

(3) The maximum sample rate was determined experimentally.

Results

Part A: D/A Conversion with R-2R Ladder Converter

(1) Students constructed the circuit as intended. After testing the circuit, the following scope images were obtained which confirm the 16 states and that the maximum voltage is 3V.

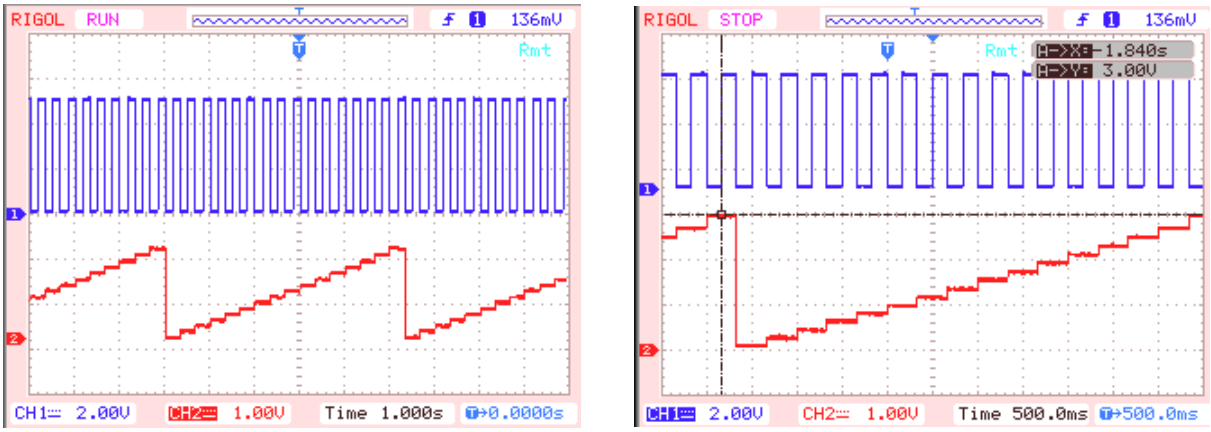

Figure 2: Scope output of the D/A converter with max output of 3V

(2) The following figure shows the plot of the output voltage of the D/A converter versus the input 4-bit word.

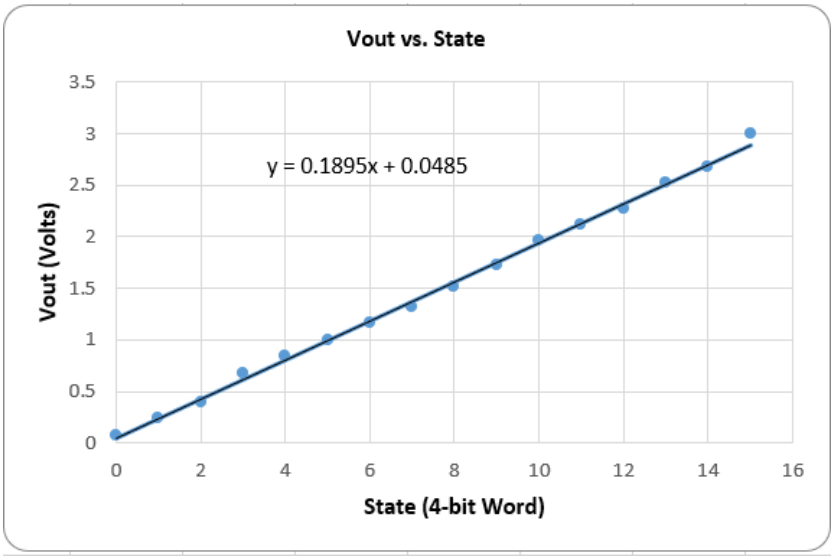

Figure 3: Plot of measured V_{out} vs. the input word state

As seen in the plot above, the best fit line is:

$$V_{out} = V_{off} + G * W$$
$$V_{out} = 0.0485 + 0.1895 * W$$

Which gives $V_{off} = 0.0485$ and $G = 0.1895$.

(3) The following table lists the relative linearity errors between the measured output voltage of the D/A converter versus the best-fit line values. Error was determined by the following equation:

$$error = \frac{V_{measured} - V_{best-fit}}{V_{best-fit}} * 100\%$$

State	Measured	Best-Fit	Error
0	0.08	0.0485	64.95%
1	0.24	0.238	0.84%
2	0.4	0.4275	6.43%
3	0.68	0.617	10.21%
4	0.84	0.8065	4.15%
5	1	0.996	0.40%
6	1.16	1.1855	2.15%
7	1.32	1.375	4.00%
8	1.52	1.5645	2.84%
9	1.72	1.754	1.94%
10	1.96	1.9435	0.85%
11	2.12	2.133	0.61%
12	2.28	2.3225	1.83%
13	2.52	2.512	0.32%
14	2.68	2.7015	0.80%
15	3	2.891	3.77%

Table 1: Table of errors between measured values and best-fit line

(4) To determine the longest settling time, which occurs when all four bits are changing (1111 to 0000), students used the scope to measure the difference between state 1111 and 0000. The settling time was found to be 8 μsec. The scope image is shown in the figure below:

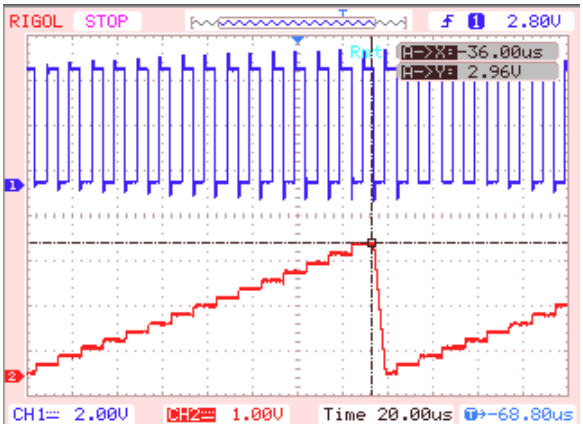

Figure 4: Scope used to determine settling time between 1111 to 0000

The rise time between each bit state transition was also measured. The following table summarizes the results:

Word	State	Rise Time
0000	0	2.6E-06
0001	1	1E-06
0010	2	1.2E-06
0011	3	1.2E-06
0100	4	1.2E-06
0101	5	8E-07
0110	6	6E-07
0111	7	1E-06
1000	8	2.2E-06
1001	9	1.8E-06
1010	10	8E-07
1011	11	1E-06
1100	12	6E-07
1101	13	8E-07
1110	14	8E-07
1111	15	6.2E-06

Table 2: Table of Rise Times for each state transition

Part B: Parallel A/D Converter

(1) See prelab for designs

(2) Shown below are the responses of each bit A2-A0 (MSB-LSB) to a ramp input:

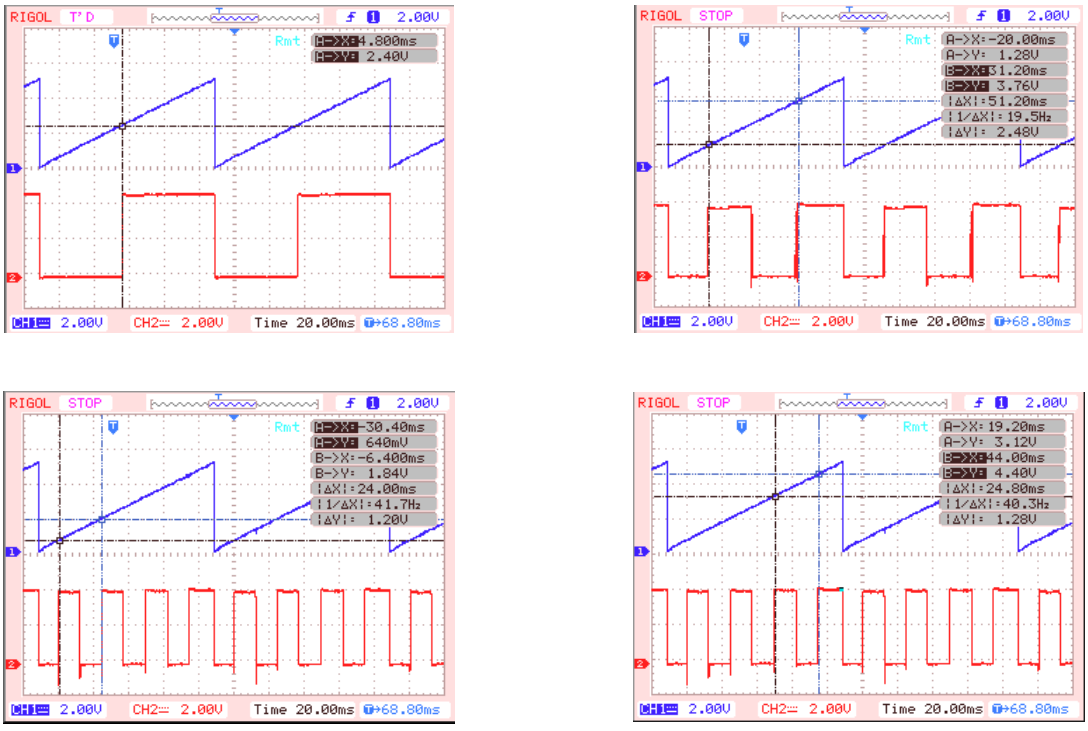

Figure 5: Output bit responses to ramp input. MSB A2 (Top Left), A1 (Top Right), LSB1 A0 (Bottom Left), LSB2 (Bottom Right)

(3) Below are oscilloscope captures of a good sample and maximum sample rate of the system, when the comparators no longer output the correct square wave in response to a 5V input:

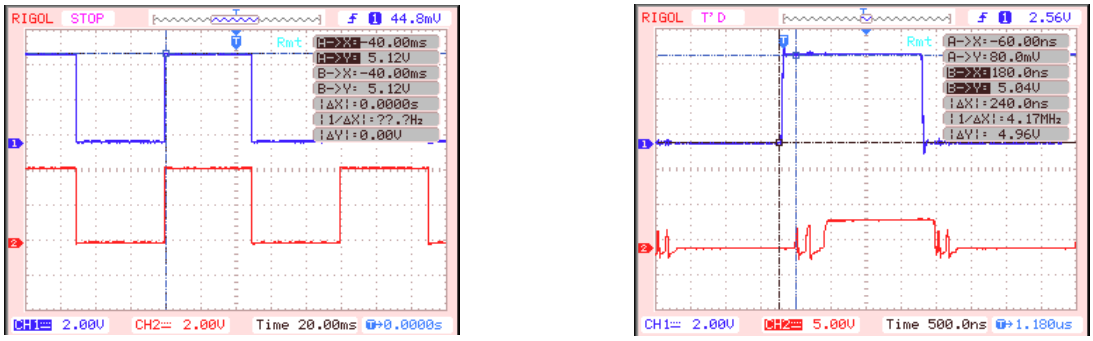

Figure 6: Good sample rate (left) and failed sample rate (right)

Discussion

Part A: D/A Conversion with R-2R Ladder Converter

(1) Figure 2 shows the output of the D/A R-2R converter. As seen in the figure on the left, the output shows each of the 16 states corresponding to 0000 all the way up to 1111. This confirmed that the converter was functioning correctly and constructed correctly because it was able to achieve 16 distinct analog voltage states.

Furthermore, the figure on the right in Figure 2 confirms that the entire circuit was constructed correctly because it shows the maximum voltage achieved at the 16th state. As seen in the figure, it is measured to be 3V which was the intended maximum voltage. This confirms that the resistances chosen in the op amp circuit were able to successfully achieve the desired output voltage.

(2) Figure 3 shows the plot of the output voltage versus each of the input word digital states. Linear regression was done to find the line of best fit. The best-fit equation was determined to be:

$$V_{out} = 0.0485 + 0.1895 * W$$

As seen in the equation, the V_{off} voltage was found to be 0.0485 by the best-fit line. This value makes sense because in theory it should be equal to zero, but voltage fluctuations resulted in a value of millivolts. This makes sense because in any system with noise and other disturbances, the off voltage will not be exactly zero.

As for the slope equal to 0.1895, this value also makes sense. The theoretical value here is 0.2 because at the maximum word state (1111) which is W = 15, 0.2*15 = 3 which is the theoretical maximum. Our best fit line slope provides a 5.25% error which is good.

(3) The errors between the measured and best line of fit averaged out at 3.2%, excluding the first state which was anomalously 65% error. However, the magnitude of difference at this state was only 3μs, so the small time value affected the percentage error. Overall the r^2 value for the best (linear) line of fit was 0.997 so, the prediction accurately reflected the actual response of the converter circuit.

(4)The first speed limitations is the LSB switch rate, since it is switched every state transition. The delay for the LSB is 8μs. The second speed limitation is the switch from state 8 (111) and state 0 (000), because it requires all three bits to change. This delay also occurs in the transition between states 3 (011) and 4 (100), which also require all bits to change simultaneously. This is most evident in Figure 4 in the accentuated time delay between state 8 and 0, where the slope is no longer vertical.

Part B: Parallel A/D Converter

(1) A voltage converter was designed to output the analog voltages needed to input into the A/D converter.

(2) Figure 5 displays the outputs of each bit in response to a low frequency ramp input. These images verify the correct operation of the converter: The A2 bit (MSB) is at 50% duty cycle corresponding to the second half of the ramp wave (higher voltages. The A1 bit is also at 50% duty cycle but at twice the frequency of the ramp wave (and A2 bit). Finally the A0 bit (LSB) occurs at even double the frequency of A1 and quadruple the frequency as A2. These are all expected as it shows that 8 binary states are being cycled through, which is correct since there are 3 bits and $2^3 = 8$.

(3) The maximum frequency was found to be 250kHz, as shown in Figure 6, when the comparators can no longer keep up with the frequency of the input and fail to output a correct wave form, tested here with a $5V_{pp}$ square wave input. In contrast, a 10Hz frequency show on the left outputs a perfectly mirrored square wave.

Conclusion

The purpose of lab 7 was to experimentally analyze, build, and test D/A and A/D converters. In the D/A converter case, we analyzed a R-2R converter technique used to translate 16 digital states (0000 to 1111) to 16 different analog values. By utilizing an op amp circuit and resistances, we were able to limit the maximum output voltage to a desired 3V. In the A/D converter case, we analyzed a circuit using 339 comparator chips and designed combinational logic to take a analog input voltage and convert it to a three bit digital output. In both cases, scope images were captured to confirm functionality and speed limitations were assessed of both converters.

Results accurately reflected what was expected and taught in lecture. Key takeaways were learning the structure and usage of different conversion circuits. This experiment also exposed students to one of the applications of the variety of digital applications for comparators. This experiment also demonstrated the importance of accuracy in design to obtain desired results and the differences that can arise between theoretical and practical responses.

References

[1] Experiment 7 – D/A and A/D Conversion Lecture Notes

[2] Rigol DM3058 User's Guide. https://www.csulb.edu/sites/default/files/groups/college-of-engineering/About/rigol-dm3058-digital-multimeter-user-guide.pdf

[3] 741 Op Amp Datasheet: http://www.ti.com/lit/ds/symlink/lm741.pdf

[4] 339 Comparitor Datasheet: http://www.ti.com/lit/ds/symlink/lm2901.pdf

[5] Professor Li