ECE 501 Digital Systems Laboratory
Experiment 9 – Counters

3-11-18

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Station 27

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Introduction:

Laboratory 9 was a practice in designing and building circuits. The objective was to think of and build a 15 bit up-counter. First it was simulated digitally on Altera Quartus, and then it was realized on the breadboard using 74LS74A edge-triggered D flip-flops. The properties of each (function, delays, etc.) were measured and to make a comparison between the theoretical simulation to the physical circuit.

Part A: Design and Simulation

Purpose:
The purpose of Part A was to ideate and come up with the initial design for the 4-bit binary ripple counter before starting to build a breadboard prototype. This served as expected results for our actual circuit.

Procedure:
1. A sketch was made on paper using ideas based off a previous digital logic assignment. It was copied into the lab notebook, and then translated into Altera Quartus II with these requirements:

a. It must count from 0 to 15 and start over at 0.
b. It must be a ripple counter.
c. It must use 74LS74A flip-flops (7474 in MAX+plus II).
d. It must include one PRESET and one CLEAR input for the counter (PRESET=SET, CLEAR=RESET). Note that each flip-flop has individual low-true inputs for PRESET and CLEAR

2. The waveform simulator was used to analyze the circuit design and make sure that it was working as intended.

Results:
1. Figure 1a below shows the design made in Altera Quartus:

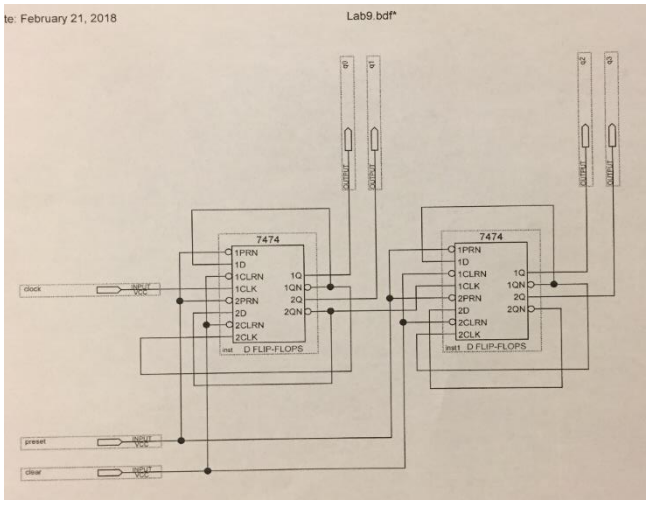


Fig1a. 4-bit binary counter schematic utilizing two 7474 IC D flip-flops in Altera Quartus

The design uses 4 74LS74A edge-triggered D flip-flops on 2 7474 IC chips. In figure 1a, the left chip, containing flip-flops 0 and 1, is connected to the right chip, containing flip-flops 2 and 3.

The CLK is the clock input to the first D flip-flop. To make the circuit count, the inverted output (QN) of the first D flip-flop (0) was tied to both its own D input and the clock input of the second D flip-flop (1). This doubled the period of the second D flip-flop's output. Making similar connections between the second (1), third (2), and fourth (3) D flip-flops caused this doubling effect to cascade with each D flip-flop, until the periods of D flip-flops 1, 2, and 3 were 2x, 4x, and 8x, respectively, the period of D flip-flop 0. After arranging the outputs of the flip-flops as $Q_3Q_2Q_1Q_0$, the resulting 4-digit number can be read in binary ranging from 0000 (0) to 1111 (15). This number updates every rising clock edge of flip-flop 0, counting sequentially in a loop from 0-15.

2. Figure 2b below shows the output of the schematic's wave form simulation:

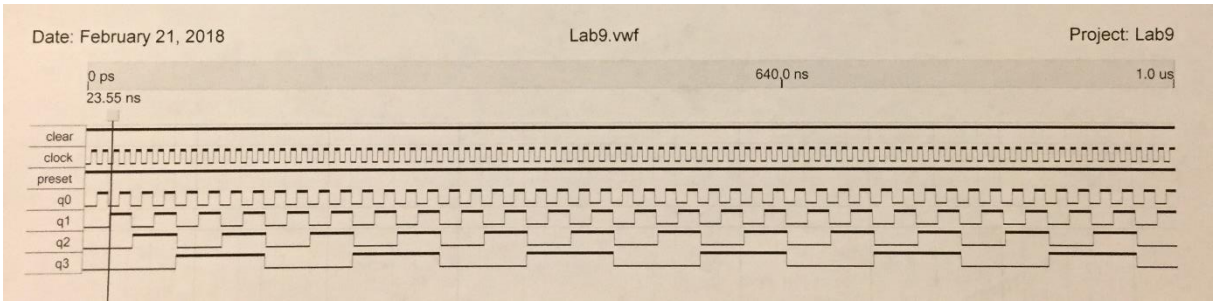


Fig1b. Waveform simulator output for 4-bit binary ripple counter schematic, 6 full periods

PRESET and CLEAR were set to HIGH in order to disable them for the duration of the simulation (they were low-true inputs). The clock was set to square wave with amplitude 5V and period 10ns.

The delay between clock edge and output update was found by measuring the time between the clock edge where each transition triggered (falling edge for this input wave) and the point of each output update. Below figure 1c shows the delay between each update:

Transition update	# Flip-Flops Changing	Delay Time (ns)
0000 >> 0001	1	1.19
0001 >> 0010	2	2.64
0010 >> 0011	1	1.19
0011 >> 0100	3	3.89
0100 >> 0101	1	1.19
0101 >> 0110	2	2.64
0110 >> 0111	1	1.19
0111 >> 1000	4	5.14
1000 >> 1001	1	1.19
1001 >> 1010	2	2.64
1010 >> 1011	1	1.19
1011 >> 1100	3	3.89
1100 >> 1101	1	1.19
1101 >> 1110	2	2.64
1110 >> 1111	1	1.19
1111 >> 0000	4	5.14

Fig1c. transition delay from clock edge to update

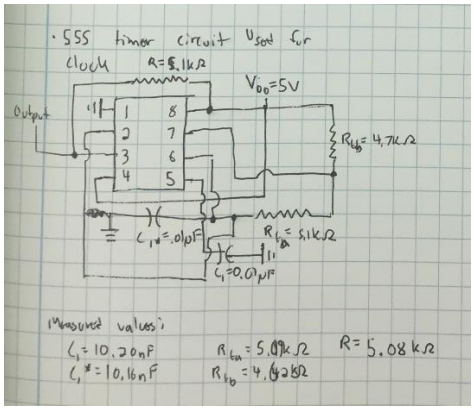
All values were found after by increasing the time scaling to a fine enough resolution. There is a trend in the data: delay time increases as the number of flip-flops changing increases. After a baseline delay of 0.2ns, adding on 1 flip-flop causes a set increase in delay time measure to be 1.25ns. This is expected since the signal each flip-flop that the signal must propagate through will increase the delay time by the same amount (since they are identical flip-flops).

Conclusion:
Designing in Altera Quartus enabled for rapid changes to be made and evaluated. The observations made were expected and successful for a 4-bit binary ripple counter, so they can serve as expected values and results for the physical realization of the circuit in Part B.

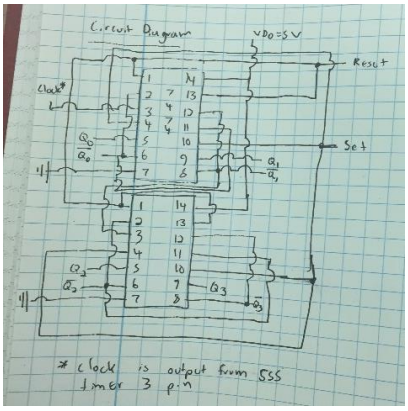
Part B: Building the Circuit

Purpose:
The purpose of Part B was to build the circuit designed and simulated in Part A, observe its functionality, and compare this to theoretical values and results obtained in Part A.

Procedure:
1. We built the 4-bit binary ripple-counter from the Altera Quartus schematic using 2 7474 D flip-flop IC's, a 555 timer (chip + resistors and capacitors), and LED's to represent outputs.



555 Timer Clock Schematic



Ripple Counter Schematic

2. The oscilloscope was used display the output waves forms of Clock, Q_0, Q_1, Q_2, and Q_3.

3. The oscilloscope was used to determine the delays measured in Part A by measuring the delay between the 50% threshold of the clock rising edge (transitions were triggered on the rising edge in the circuit as opposed to falling edge in the simulation) and the 50% threshold of each Q_i rising edge.

Results:
1. We built both the 555 Timer and the Ripple Counter above using the schematics and pin connections shown above. Using the measured values of the capacitors and resistors, we calculated and set the period of clock signal to be 100.69μs, or 100,000x larger than the minimum transition delay we found in Part A. As expected, the LED's lit in the correct sequence and combinations, confirming that we put the circuit together correctly.

2. The oscilloscope could not display all waveforms at once, so two images were taken (the first of clock, Q_0, and Q_1. The second of Q_1, Q_2, and Q_3). Identical scaling and positions were carefully maintained so that the images could be superimposed onto one another to create a single, full display. Figure 2a below displays the clock signal, Q_0, Q_1, Q_2, and Q_3 outputs:

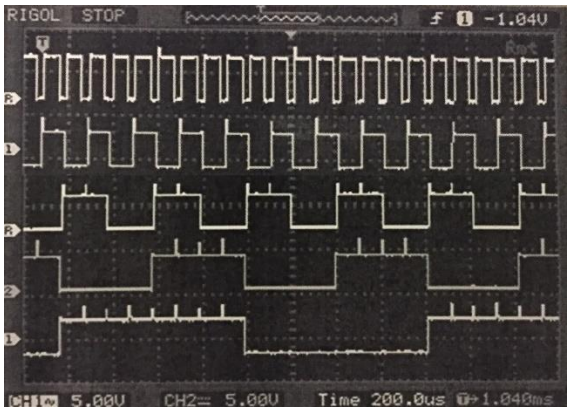


Fig 2a. (top to bottom) CLK, Q_0, Q_1, Q_2, and Q_3 signals, oscilloscope display

Voltage and time scalings were set to 5V/division 200µs/division, respectively. Though this confirmed that the counter was working properly (followed the predicted behavior is Part A concerning relative lengths of periods), the 555 Timer period was measured at 85µs rather that the 100µs calculated. This is could well be due to an extra 1kΩ load resistor placed across the 555 Timer to stabilize the output signal.

3. Figure 2b below shows the time delay Δx between the 50% threshold of CLK (average of V_{ClkMin} and V_{ClkMax}) and 50% threshold of Q_0 (average of V_{Q_0Min} and V_{Q_0Max}). This delay was measured between corresponding rising edges.

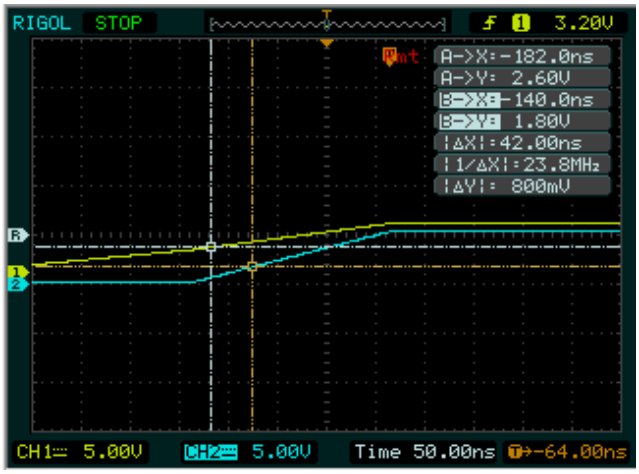


Fig 2b. 42ns delay between CLK and Q_0 signals, scaling: 5V/div and 50ns/div

This process was repeated between clock and Q_1, Q_2, and Q_3 to produce the figure 2c:

Output	50% Threshold (V)	Δx between Clock and Output (ns)
Clock	2.6	n/a
Q_0	1.8	42.0
Q_1	2.0	52.1
Q_2	2.0	70.7
Q_3	2.1	78.3

Fig 2c. Table of delays between 50% thresholds clock and Q_1, Q_2, and Q_3

This data is mostly expected. The large gap between Q_1 and Q_2 is when the signal left the first 7474 IC to enter the second 7474 IC. Not counting this gap, there is a fairly close delay between successive flip-flop outputs of 10.1ns in the first IC and 7.6ns in the second IC. There is also a higher baseline delay that could be due to the internal resistance caused by wires from 555 Timer to the flip-flop's CLK input.

Overall, these delays are much larger than the simulated delays, but the behaviors were as expected: total delay increased with each flip-flop added, and this added delay was roughly the same amount per flip-flop. This was especially good due to the time scale of nano-seconds.

Conclusion: The schematic in Altera Quartus was successfully converted into an actual circuit. Though resistance of wires and other non-ideal factors increased observed delays, the trends and behaviors of the physical circuit matched those of the simulated circuit in Part A.

Overall:

Laboratory 9 went through the entire design process, from paper sketch, to digital modelling and simulation, to physically building and testing of a 4-bit binary ripple-counter. Analysis was conducted during simulations and post-build to compare values and trends. The digital simulation provided an ideal analysis of the circuit, and the physical circuit gave a real analysis.

The real analysis had longer delays due to internal resistance of wires and other non-ideal conditions, but its overall behaviors were the same as the ideal circuit. The total delay from clock edge increased with each added flip-flop by approximately the same amount per flip-flop.

Also experienced in the lab were physical limitations of the oscilloscope – both the display and knob control suffered from lack of resolution, as the measurements that were being taken were a little bit too fine.

References:

[1] 555 Timer schematic and equations - https://courseweb.pitt.edu/bbcswebdav/pid-24291878-dt-content-rid-23464842_2/courses/2184_UPITT_ECE_0501_SEC1010/555_timer.jpg

[2] 7474 Schematic - https://courseweb.pitt.edu/bbcswebdav/pid-24291878-dt-content-rid-23464850_2/courses/2184_UPITT_ECE_0501_SEC1010/7474.pdf